NBS SPECIAL PUBLICATION 400-6

U.S. DEPARTMENT OF COMMERCE / National Bureau of Standards

Semiconductor Measurement Technology:

Microelectronic Test Patterns: An Overview

NATIONAL BUREAU OF STANDARDS

The National Bureau of Standards[1] was established by an act of Congress March 3, 1901. The Bureau's overall goal is to strengthen and advance the Nation's science and technology and facilitate their effective application for public benefit. To this end, the Bureau conducts research and provides: (1) a basis for the Nation's physical measurement system, (2) scientific and technological services for industry and government, (3) a technical basis for equity in trade, and (4) technical services to promote public safety. The Bureau consists of the Institute for Basic Standards, the Institute for Materials Research, the Institute for Applied Technology, the Institute for Computer Sciences and Technology, and the Office for Information Programs.

THE INSTITUTE FOR BASIC STANDARDS provides the central basis within the United States of a complete and consistent system of physical measurement; coordinates that system with measurement systems of other nations; and furnishes essential services leading to accurate and uniform physical measurements throughout the Nation's scientific community, industry, and commerce. The Institute consists of a Center for Radiation Research, an Office of Measurement Services and the following divisions:

Applied Mathematics — Electricity — Mechanics — Heat — Optical Physics — Nuclear Sciences[2] — Applied Radiation[2] — Quantum Electronics[3] — Electromagnetics[3] — Time and Frequency[3] — Laboratory Astrophysics[3] — Cryogenics[3].

THE INSTITUTE FOR MATERIALS RESEARCH conducts materials research leading to improved methods of measurement, standards, and data on the properties of well-characterized materials needed by industry, commerce, educational institutions, and Government; provides advisory and research services to other Government agencies; and develops, produces, and distributes standard reference materials. The Institute consists of the Office of Standard Reference Materials and the following divisions:

Analytical Chemistry — Polymers — Metallurgy — Inorganic Materials — Reactor Radiation — Physical Chemistry.

THE INSTITUTE FOR APPLIED TECHNOLOGY provides technical services to promote the use of available technology and to facilitate technological innovation in industry and Government; cooperates with public and private organizations leading to the development of technological standards (including mandatory safety standards), codes and methods of test; and provides technical advice and services to Government agencies upon request. The Institute consists of a Center for Building Technology and the following divisions and offices:

Engineering and Product Standards — Weights and Measures — Invention and Innovation — Product Evaluation Technology — Electronic Technology — Technical Analysis — Measurement Engineering — Structures, Materials, and Life Safety[4] — Building Environment[4] — Technical Evaluation and Application[4] — Fire Technology.

THE INSTITUTE FOR COMPUTER SCIENCES AND TECHNOLOGY conducts research and provides technical services designed to aid Government agencies in improving cost effectiveness in the conduct of their programs through the selection, acquisition, and effective utilization of automatic data processing equipment; and serves as the principal focus within the executive branch for the development of Federal standards for automatic data processing equipment, techniques, and computer languages. The Institute consists of the following divisions:

Computer Services — Systems and Software — Computer Systems Engineering — Information Technology.

THE OFFICE FOR INFORMATION PROGRAMS promotes optimum dissemination and accessibility of scientific information generated within NBS and other agencies of the Federal Government; promotes the development of the National Standard Reference Data System and a system of information analysis centers dealing with the broader aspects of the National Measurement System; provides appropriate services to ensure that the NBS staff has optimum accessibility to the scientific information of the world. The Office consists of the following organizational units:

Office of Standard Reference Data — Office of Information Activities — Office of Technical Publications — Library — Office of International Relations.

---

[1] Headquarters and Laboratories at Gaithersburg, Maryland, unless otherwise noted; mailing address Washington, D.C. 20234.
[2] Part of the Center for Radiation Research.
[3] Located at Boulder, Colorado 80302.
[4] Part of the Center for Building Technology.

Semiconductor Measurement Technology:

Microelectronic Test Patterns: An Overview

Martin G. Buehler

Electronic Technology Division
Institute for Applied Technology
U.S. National Bureau of Standards
Washington, D.C. 20234

+. Special publication no. 400-6

Jointly sponsored by:
The Defense Advanced Research Projects Agency,
The Defense Nuclear Agency, and
The National Bureau of Standards

U.S. DEPARTMENT OF COMMERCE, Frederick B. Dent, *Secretary*

NATIONAL BUREAU OF STANDARDS, Richard W. Roberts, *Director*

Issued August 1974

Library of Congress Cataloging in Publication Data

Buehler, Martin G.
Microelectronic test patterns: An overview.

(NBS Special Publication 400-6)
"Jointly sponsored by the Defense Advanced Research Projects Agency, the Defense Nuclear Agency, and the National Bureau of Standards."
Supt. of Docs. No.: C 13.10:400.6
1. Integrated circuits—Testing. 2. Electronic apparatus and appliances—Testing. I. United States. Defense Advanced Research Projects Agency. II. United States. Defense Nuclear Agency. III. United States. National Bureau of Standards. IV. Title. V. Series: United States. National Bureau of Standards. Special Publication 400-6.
QC100.U57 No. 400-6 [TK7874] 389'.08s [621.381'73]
74-13001

National Bureau of Standards Special Publication 400-6

Nat. Bur. Stand. (U.S.), Spec. Publ. 400-6, 24 pages (Aug. 1974)

CODEN: XNBSAV

U.S. GOVERNMENT PRINTING OFFICE
WASHINGTON: 1974

For sale by the Superintendent of Documents, U.S. Government Printing Office, Washington, D.C. 20402 (Order by SD Catalog No. C13.10:400-6). Price 60 cents.

CONTENTS

FIGURE CAPTIONS

TABLE

Microelectronic Test Patterns: An Overview*

Martin G. Buehler

ABSTRACT

The test patterns considered are those designed by the physical electronics engineer to evaluate fabrication processes rather than those designed by the microcircuit designer. The evaluation of fabrication processes can reveal if a process is under control and can indicate the stability and reliability of the resulting microcircuit. This evaluation is in essence an evaluation of a microcircuit's material characteristics, for process control and reliability depend ultimately on the right atoms being in the right places.

Various material analysis test structures are described, such as resistors, MOS capacitors, and gated *p-n* junctions along with the material parameters that can be derived from each. These test structures are illustrated by the NBS-2 test pattern, and its use in process control is described. Examples are given which span the range from those structures which are amenable to production testing to those which require an advanced measurement capability. In addition test structures are discussed with regard to their usability; this encompasses their size, sensitivity, correlation, contacting schemes, testability, and packaging. Test structures must be properly designed so that desired parameters are measured. In this regard various design aspects such as metal taps and diffused taps are mentioned. Finally the role of NBS in evaluating and designing test patterns is discussed.

Key words: Integrated circuits; microelectronic test patterns.

I. INTRODUCTION

Microelectronic test patterns are meant to facilitate the fabrication of more reliable and lower cost microcircuits [1,2,3,4,5]. If they are to be effective in meeting this objective, their presence must not impede the production of the microcircuits. They must allow the user to pin-point problem areas quickly so that timely corrective action can be taken. This means that test structures must be designed to consume a minimum of space, be easily fabricated, tested, and analyzed, and speak directly to problem areas. A significant effort is now planned by NBS to develop various test structures and encourage their implementation in production processes. The reason for this effort now is that test patterns can affect both the yield and reliability at the wafer level and they can be used to bridge the buyer/seller interface by giving the buyer confidence in the product he has purchased.

To effectively implement test patterns, the associated test apparatus, data acquisition and reduction systems, and mathematical models must be developed. In addition, the product engineer must be convinced to devote some of his precious space on the wafer to test patterns. This paper focuses on the use and design of test patterns and considers only in passing the total environment in which the pattern must function. In Section II, a description is given of the term, test pattern. Sections III and IV are devoted to how test patterns are used and the information that can be derived from them. A test pattern developed at NBS is described in Section V and two test structures from this pattern are discussed in detail to illustrate its various uses. The design and evaluation of test patterns is discussed in Section VI, and finally the response of NBS to the industrial need is described in Section VII.

---

*Based on a talk presented at the Mini-Symposium on Semiconductor Test Patterns sponsored by the ASTM Committee F-1 on Electronics in New Orleans, January 15, 1974.

II. ATTRIBUTES OF TEST PATTERNS

Four arrangements of test structures on a wafer have been identified. The first arrange arrangement consists of a test wafer completely covered with test structures and used for an experimental study of the process. The second arrangement consists of test structures placed on the periphery of every microcircuit chip and used for process control. In the last two categories the production wafer contains test chips which replace the entire microcircuit chip at selected points. These test chips allow across-the-wafer measurements or quadrant measurements as illustrated in figure 1. The third arrangement consists of a material analysis test chip used for process control and reliability analysis. The final arrangement consists of an expanded metallization test chip where the microcircuit metallization has been altered to allow access to circuit elements such as transistors and resistors. These chips are used in circuit design and yield analysis.

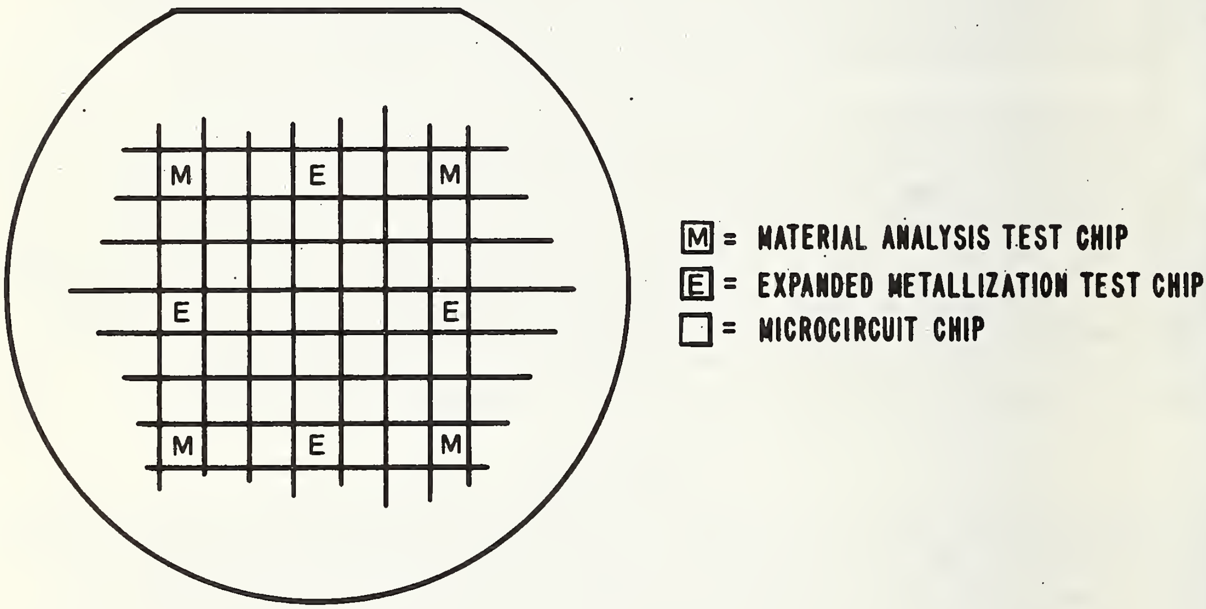


Figure 1. Test chips distributed among microcircuits on a production wafer.

The kinds of test regions may vary from clear areas for etch control to patterned areas utilized in various ways. Alignment and resolution patterns are used in photoresist operations and for etch control. Process control structures fall into two categories: those that can be probed before wafers are metallized and those probed after metallization. Those probed before metallization are used to provide rapid feedback to the process. For example, the gain of a transistor can be brought into specification by additional heat cycles prior to metallization. Those structures probed after metallization are used to monitor the process by giving overall trends and allowing for longer range corrective action. Such structures are typically sheet resistors, contact resistors, metal continuity resistors, test diodes and test transistors. These process control structures evaluate the material characteristics of microcircuits. In contrast, circuit and device oriented test structures are useful to the design engineer since they give him information relative to the overall design. They consist of the various resistors, capacitors, diodes, and transistors found in the microcircuit. The final category consists of reliability and failure analysis structures. They are special structures such as MOS capacitors and metal step coverage resistors. The testing environment for these structures is meant to induce failure modes. As such, extreme temperatures and extreme current pulses may be used.

III. USE OF TEST PATTERNS

In high volume production, operating in a steady state mode, the use of test patterns traditionally plays a relatively minor role, for process control is achieved by other empirical means. However, in such an environment, test patterns can provide early warning that process controls may be deteriorating. In low volume production, where processes must be changed rapidly, they can help to quickly bring the process within specification. In the production of custom microcircuits [6], the process may remain the same, but different photomasks are used to suit customer circuit requirements. Here test patterns provide a common link between a variety of circuits insuring that process control has been maintained. The concept of control through test patterns also proves useful when comparing circuits fabricated at different facilities.

Test patterns can be used to judge the potential reliability of a microcircuit chip and to assess the causes of failure. The MOS capacitor bias-temperature stress test is an example [7] of how a test structure can be used to predict reliability. Test structures, such as test transistors located on the periphery of a microcircuit, can prove invaluable in diagnosing a returned circuit.

IV. INFORMATION DERIVED FROM TEST PATTERNS

Typical information derivable from various test patterns is summarized below. The list progresses from the least sophisticated structures to advanced test structures, such as the charged coupled device (CCD) [8] and NAND gate. Material parameters such as sheet resistance, lifetime, and defect and dopant densities are listed along with various device parameters.

1. Sheet Resistor: sheet resistance.
2. Al/Si Contact Resistor: contact resistance.
3. Bulk Resistor: bulk resistivity, back side contact resistance.
4. Metallization Resistor: sheet resistance, step coverage resistance.
5. MOS Capacitor: dopant density, defect density, fixed oxide charge density, fast interface state density, carrier lifetime, defect identity, oxide dielectric constant, oxide thickness, oxide breakdown voltage.
6. Gated *p-n* Junction: dopant density profile, defect density profile, surface recombination velocity, carrier lifetime, defect identity, breakdown voltage.
7. Bipolar Transistor: base width, effective base dopant density, saturation voltage, breakdown voltages, offset voltage.
8. MOSFET: threshold voltage, conduction factor, charge spreading activation energy.
9. CCD: fixed oxide charge density, fast interface state density.
10. NAND Gate: propagation delay.

This list illustrates the wealth of information that can be gleaned from these test structures.

V. A TEST PATTERN USED AT NBS

The test pattern that NBS is currently using [9] is shown in figure 2; the dimensions of each test structure are given in the appendix. It consists mainly of sheet resistors, contact resistors, MOS capacitors, and gated *p-n* junctions which are listed in table 1.

Table 1 — Planar Test Structures

Number	Test Structure	Dimension,[a] mil
1	Gated circular base-collector junction with diffused channel stop	D = 6
2	Ungated circular base-collector junction with diffused channel stop	D = 6
3	Ungated square base-collector junction with diffused channel stop	S′ = 5
4	Gated square base-collector junction with diffused channel stop	S′ = 18
5	Ungated circular base-collector junction with diffused channel stop	D = 20
6	Gated circular base-collector junction with diffused channel stop	D = 20
7	Gated circular base-collector junction (small emitter) with diffused channel stop	D = 20
8	Gated circular base-collector junction (large emitter) with diffused channel stop	D = 20
9	Gated circular base-collector junction with diffused channel stop	D = 60
10	MOS capacitor over collector with field plate and diffused channel stop	D = 6
11	MOS capacitor over collector with field plate and diffused channel stop	D = 20
12	MOS capacitor over collector with distant field plate and diffused channel stop	D = 20
13	MOS capacitor over base without field plate and diffused channel stop	D = 20
14	Base sheet resistor	
15	Emitter sheet resistor	
16	Metal-to-base contact resistor	
17	Metal-to-emitter contact resistor	
18	Collector resistor	
19	Base-under-the-emitter sheet resistor (tetrode transistor)	
20	Hall effect pattern	
21	Alignment marker	

[a] D = diameter of a circle, S′ = side of a square. Tolerances should be held to ±0.1 mil. If metric dimensions are desired the diameters should be 0.15 mm (for structures numbered 1, 2, 10), 0.5 mm (5-8, 11-13), and 1.5 mm (9), and the sides should be 0.13 mm (3) and 0.46 mm (4); all tolerances should be held to ±0.002 mm.

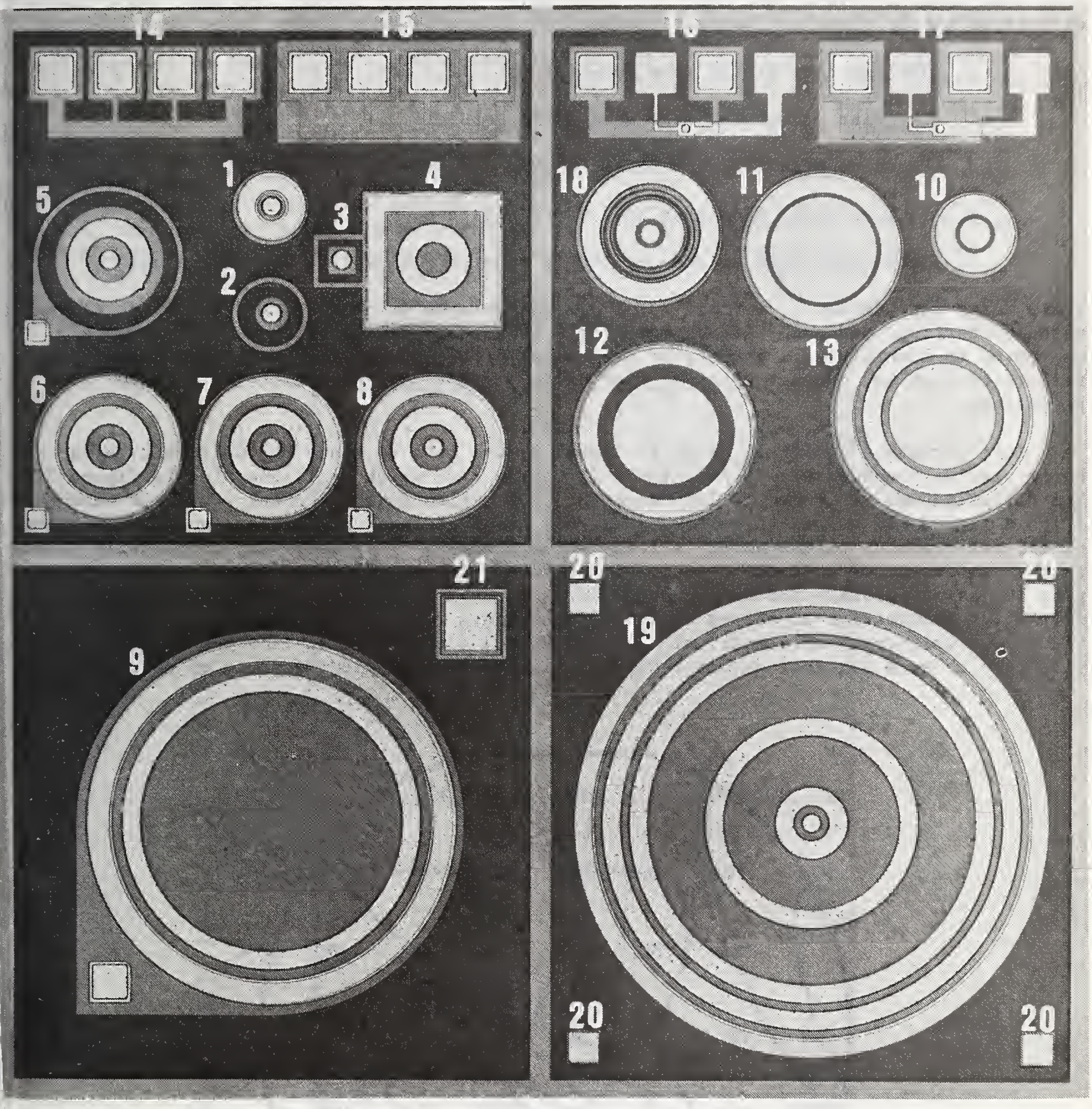


Figure 2. Test pattern, NBS-2, for characterizing the electrical properties of silicon MOS capacitors and *p-n* junctions. (The 21 elements are identified in table 1. The overall pattern is 200 mils (5.08 mm) on a side.)

The design objectives of this pattern were two fold. First, it was intended to identify problem areas within our in-house fabrication facility. Second, it was intended to allow us to develop various measurement methods. For example, *p-n* junctions with various diameters have been used to develop the junction CV impurity profiling method. To meet these design objectives and to simplify the fabrication, the following four design rules were observed.

1. Minimum line widths were one-half mil (12.7 μm).

2. Circular geometries were used where possible.

3. Expanded metallization contacts were avoided where possible.

4. In-line probe pads were used where possible.

5. Metal pads were no smaller than a square, 4 mils (102 μm) on a side.

These rules were chosen to minimize problems encountered in bonding, probing, mask alignment, pinhole shorting, and mathematical modeling. This test pattern has been of immediate use to us in identifying a variety of processing problems such as non-uniform diffusions, failure to etch out contact windows, poor oxide quality, and high backside contact resistance.

Test structure number 14, seen in figure 2, was used to study the uniformity of a boron nitride predeposition and drive-in diffusion [10] which is illustrated in figure 3. The diffusion was performed at 1000°C and had a junction depth of about 1 μm. As shown in this figure the across-the-wafer variations are such that the sample standard deviation of all measurements on the wafer is less than 2 percent. This wafer map graphically illustrates the degree of control possible with a boron nitride diffusion source. Wafer mapping of various process and device parameters has proven to be of immense importance in developing fabrication processes which produce wafers with uniform electrical characteristics. The uniformity of electrical characteristics across a wafer is a key both to high yield and to such critical requirements as predictable radiation response of microcircuits.

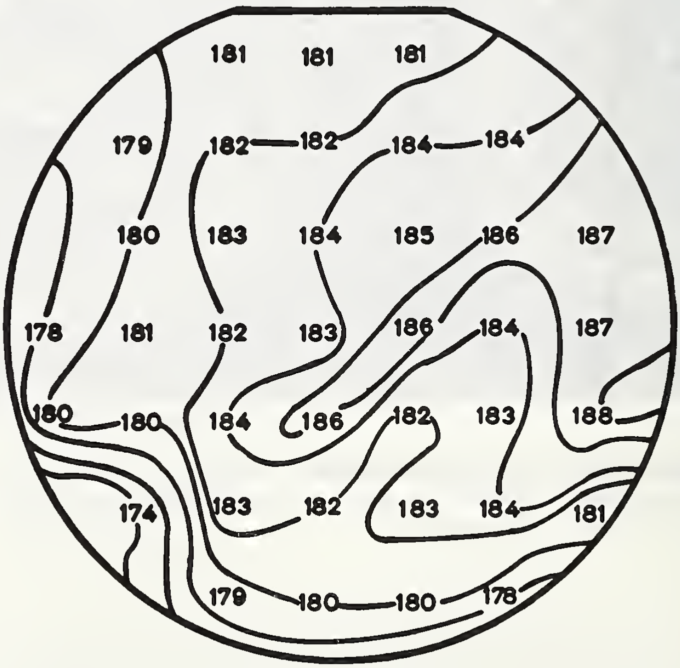


Figure 3. The base sheet resistance (Ω/□) across a 1.5-inch (3.8-cm) diameter silicon wafer. Test structure number 14, shown in figure 2, was used.

The testing and probing apparatus used to acquire the data shown in figure 3 is quite simple. As an illustration of a more advanced measurement, consider the detection and identification of defect centers in a *p-n* junction. These centers can govern the leakage current and carrier lifetime of semiconductor devices. We are currently developing a measurement method [11] that uses the thermally stimulated current and capacitance response of a *p-n* junction to identify the atomic nature of defect centers and to determine their density [12]. As shown in figure 4, a reverse biased p^+-n junction is heated rapidly from liquid nitrogen to room temperature and at the appropriate temperature, about 225 K, the junction begins to leak, in this case due to the presence of gold in the junction. The experiment was performed at three different heating rates as indicated on the figure. The particular shape of the current response identifies the defect center as gold. The shift in the capacitance response indicates that the density of gold atoms is about 1×10^{13} cm^{-3}. Measurements of this kind are in an early stage of development, but show great promise of having considerable impact on process control and contamination analysis. Recently [13] we have shown that defects can be identified in MOS capacitors as well as in *p-n* junctions. Automation of the measurements will allow wafer mapping of contaminants, which is a key to sophisticated process control.

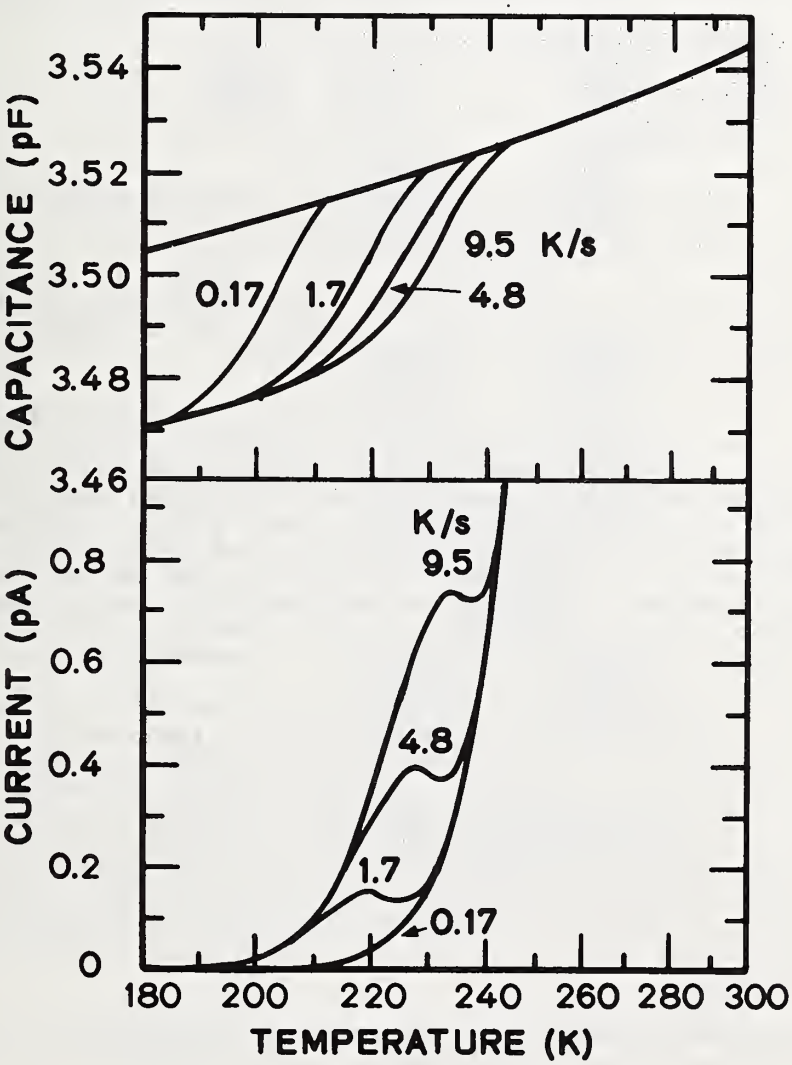


Figure 4. The thermally stimulated current and capacitance measurement of a gold doped p^+n silicon junction. Test structure number 6, shown in figure 2, was used.

VI. DESIGN AND TESTING CONCERNS

When designing test patterns, the alignment tolerances and line widths should be as generous as possible to minimize fabrication problems. One does not want to make the fabrication of the test vehicle more difficult than the fabrication of the microcircuit. However, there are structures, such as the metal step coverage resistor, where line widths should be as small, if not smaller, than those used in the microcircuit so as to exaggerat failure modes.

Another concern is the size of the test pattern; the rule, *the smaller the better*, must generally be followed. But this must be tempered by other considerations such as sensitivity and the effect of the periphery [14] on measurements. Also the designer must consider various probe-contacting schemes such as a metal probe pad in direct contact with the silicon or a metal probe pad resting on top of the oxide. This latter scheme, known as an expanded contact, has stray capacitance and may induce an inversion layer in the silicon under the contact. These can be undesirable complications.

With regard to electrical testing, the kind of test structure chosen will depend on the nature of the test. Electrical testing can be categorized as follows:

1. DC, AC or functional,
2. Automatic or manual,
3. Wafer or package.

One would like to design a structure whose testing is simple and rapid. In addition the data reduction should be straightforward and uncomplicated. This calls for the developmen of simple structures and the appropriate mathematical models.

The correlation of test pattern results with characteristics of the microcircuit is an area that needs a great deal of work. A data base must be developed for each test structure to establish the viability of the test structure.

Shown in figure 5 is an example of one kind of test structure development that is needed. Various test structures are possible for measuring the sheet resistance of diffus layers. The structure shown in figure 5A suffers because the metal taps act as shorting regions giving too low a sheet resistance. In addition the sheet resistance calculation depends on the L/W ratio. The structure shown in figure 5B is an improvement in that the sheet resistance is correctly determined, but the sheet resistance calculation again depends on the L/W ratio. The structure in figure 5C is a further improvement for now the L/W ratio is not needed to interpret the measurement [15]. Another advantage of this structure is that the main diffusion region can be the same size as the actual device. This means that the true sheet resistance value of a transistor base can be measured.

Measurements using the structures in figures 5A, 5B, and 5C are satisfactory for p-diffusions into n-substrates where the surfaces of the n-substrates are usually accumula due to positive charge in the oxide and phosphorus pile-up effects during oxidization. However, when substrates are p-type, these structures may fail to provide correct sheet resistance values if the surfaces of the substrates are inverted (channeled) due to positi charge in the oxide and boron depletion effects during oxidization. To overcome the effec of channeling, the structure shown in figure 5C is first rearranged as shown in figure 5D and then a gate and channel stop are added as shown in figure 5E. A cross section of this structure is shown in figure 5F. In figure 5E the periphery of the main diffused region i covered by a gate resting on oxide. By adjusting the potential on this gate, surface char nels can be eliminated.

Various other test structures need to be explored in a similar manner keeping in minc the various design trade-offs already discussed.

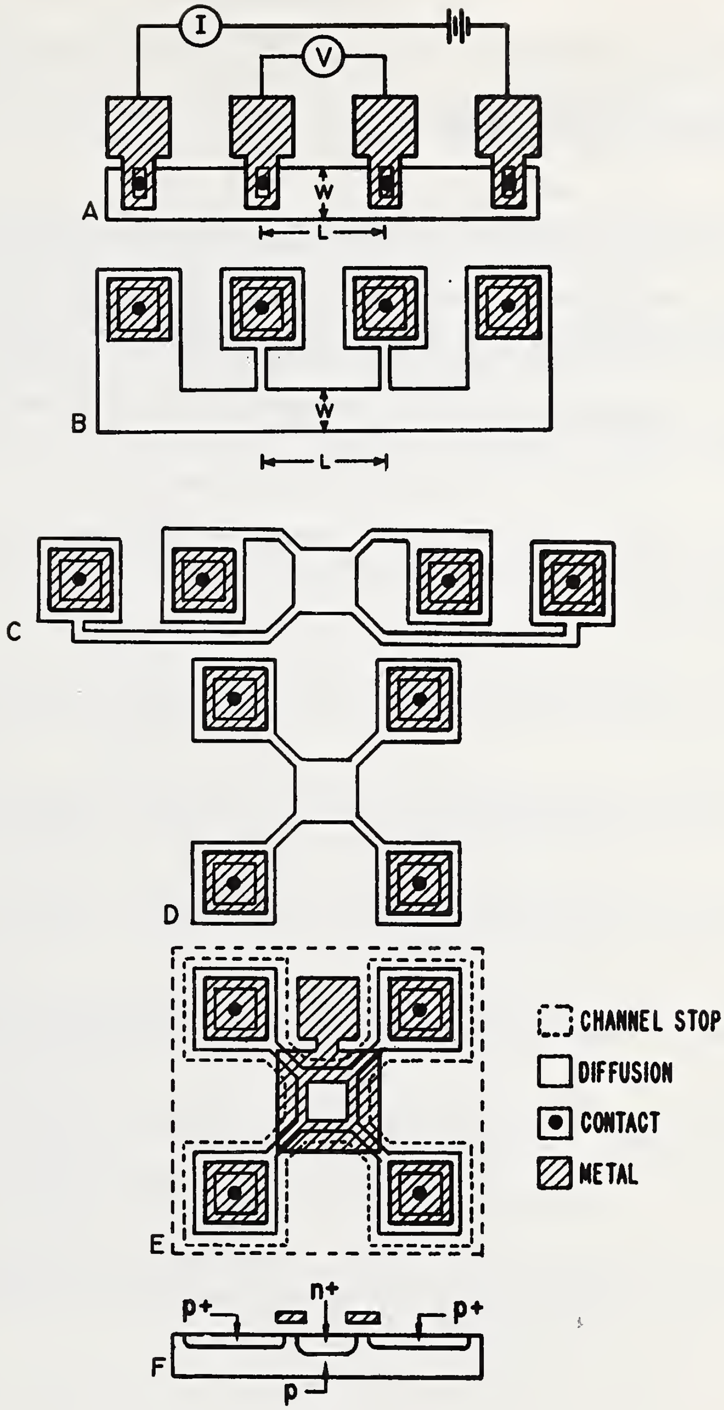


Figure 5. Various diffused layer sheet resistors having a variety of Kelvin contact schemes.

VII. THE RESPONSE OF NBS TO THE NEED

To assist the industry in the timely and effective application of test patterns, NBS has undertaken an effort to review and evaluate test structures for use in the production of cost effective, highly reliable microelectronic components. Specific goals established for this effort include:

1. Identification of those structures useful in process control.

2. Analysis and intercomparison of selected structures.

3. Development of measurement methods for use with these structures.

4. Development of miniature test structures.

5. Correlation of results from test structures with microcircuit characteristics.

6. Development of test structure catalogs.

Among other benefits, this effort is intended to enable NBS to advise the industry and government agencies regarding the trade-offs encountered in using a particular class of test structures.

REFERENCES

1. Penney, W. M., and Lau, L., eds, *MOS Integrated Circuits,* (Van Nostrand-Reinhold Co., New York, 1972).

2. Sahni, R. J., Use of Test Patterns in Evaluating the Reliability of Integrated Circuits, *8th Annual Proceedings, Reliability Physics Symposium 1970,* pp. 226-231, IEEE Catalog No. 70C59-PHY.

3. van Beck, H. W., MOS/LSI Circuit Design: Designing-In Reliability, *10th Annual Proceedings, Reliability Physics Symposium 1972,* pp. 36-41, IEEE Catalog No. 72CH0628-8-PHY.

4. Test Methods and Procedures for Microcircuit Line Certification, NHB5300-4(3D), May 1971 edition, National Aeronautics and Space Administration.

5. Schlegel, E. S., and Schnable, G. L., The Application of Test Structures for the Study of Surface Effects in LSI Circuitry, *IEEE Trans. on Electron Devices* ED-16, 386-393 (1969).

6. Ref. 1, pp. 442-444.

7. Gray, P. V., The Silicon-Silicon Dioxide System, *Proc. IEEE* 57, 1543-1551 (1969).

8. Amelio, G. F., Charged-Coupled Devices, *Scientific American* 230, 22-31 (February 1974).

9. Bullis, W. M., ed., Methods of Measurement for Semiconductor Materials, Process Control, and Devices, Quarterly Report, January 1 to March 31, 1973, NBS Technical Note 788 (August 1973) pp. 16-17.

10. Bullis, W. M., ed., Methods of Measurement for Semiconductor Materials, Process Control, and Devices, Quarterly Report, April 1 to June 30, 1974, NBS Technical Note 806 (November 1973) pp. 41-43.

11. Bullis, W. M., ed., Methods of Measurement for Semiconductor Materials, Process Control, and Devices, Quarterly Report, April 1 to June 30, 1973, NBS Technical Note 806 (November 1973) pp. 13-16.

12. Buehler, M. G., Thermally Stimulated Measurements: The Characterization of Defects in Silicon *p-n* Junctions, *Semiconductor Silicon 1973,* H. R. Huff and R. R. Burgess, eds., pp. 549-560 (Electrochemical Society, Princeton, N. J., 1973).

13. Bullis, W. M., ed., Semiconductor Measurement Technology, Quarterly Report, July 1 to September 30, 1973, NBS Special Publication 400-1 (March 1974) pp. 16-19.

14. Buehler, M. G., Peripheral and Diffused Layer Effects on Doping Profiles, *IEEE Trans. Electron Devices* ED-19, 1171-1178 (1972).

15. van der Pauw, L. J., A Method of Measuring the Resistivity and Hall Coefficient on Lamellae of Arbitrary Shape, *Philips Research Reports,* 13, 1-9 (1958).

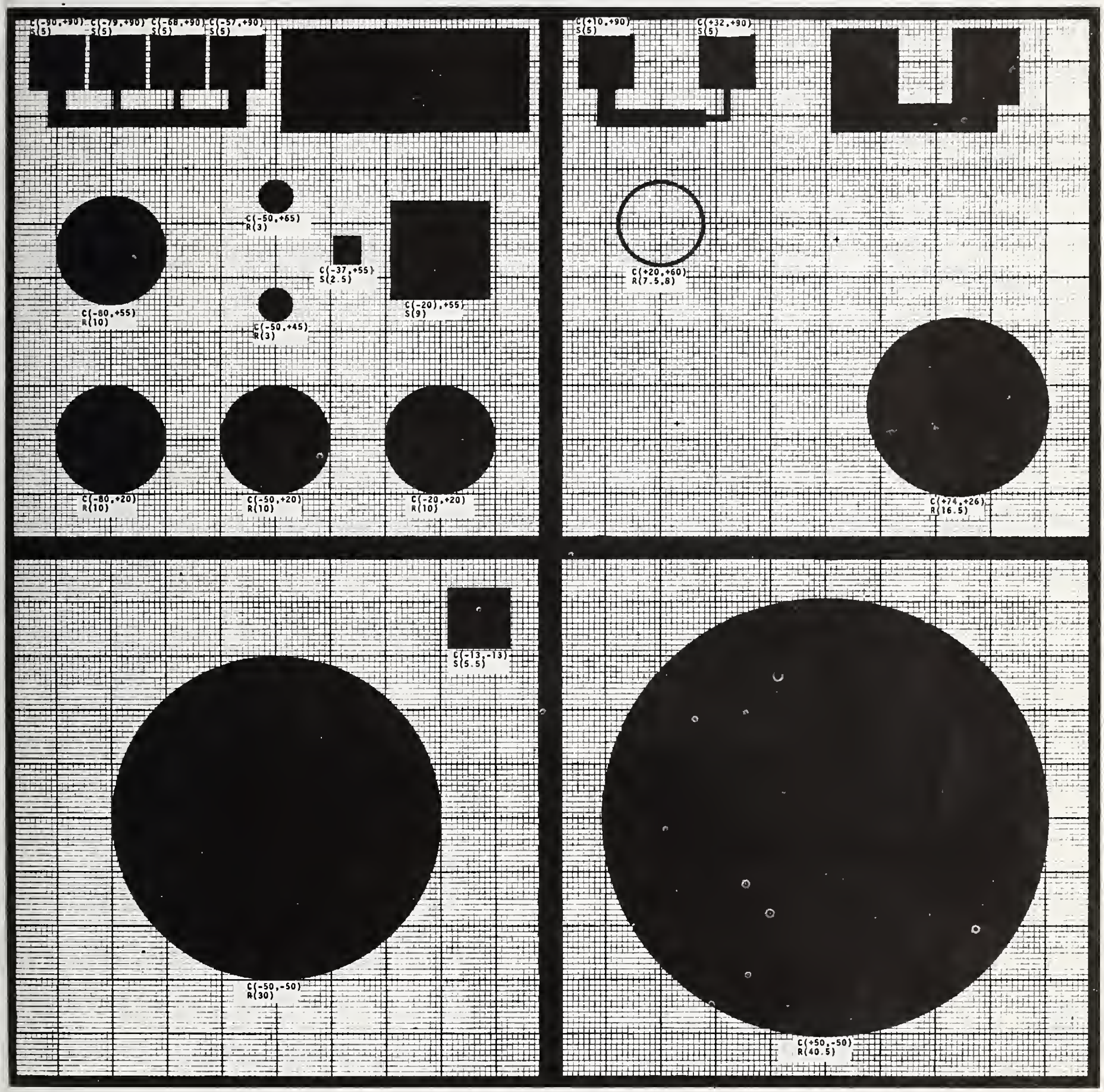
APPENDIX

TEST PATTERN NBS-2

Note: All dimensions in mils. Center of mask is taken as (0,0); horizontal coordinate is given first followed by vertical coordinate. One square equals one mil. Lines not on grid lines are halfway between grid lines. C = Center. R = Radius. S = Distance from center C to one side of square.

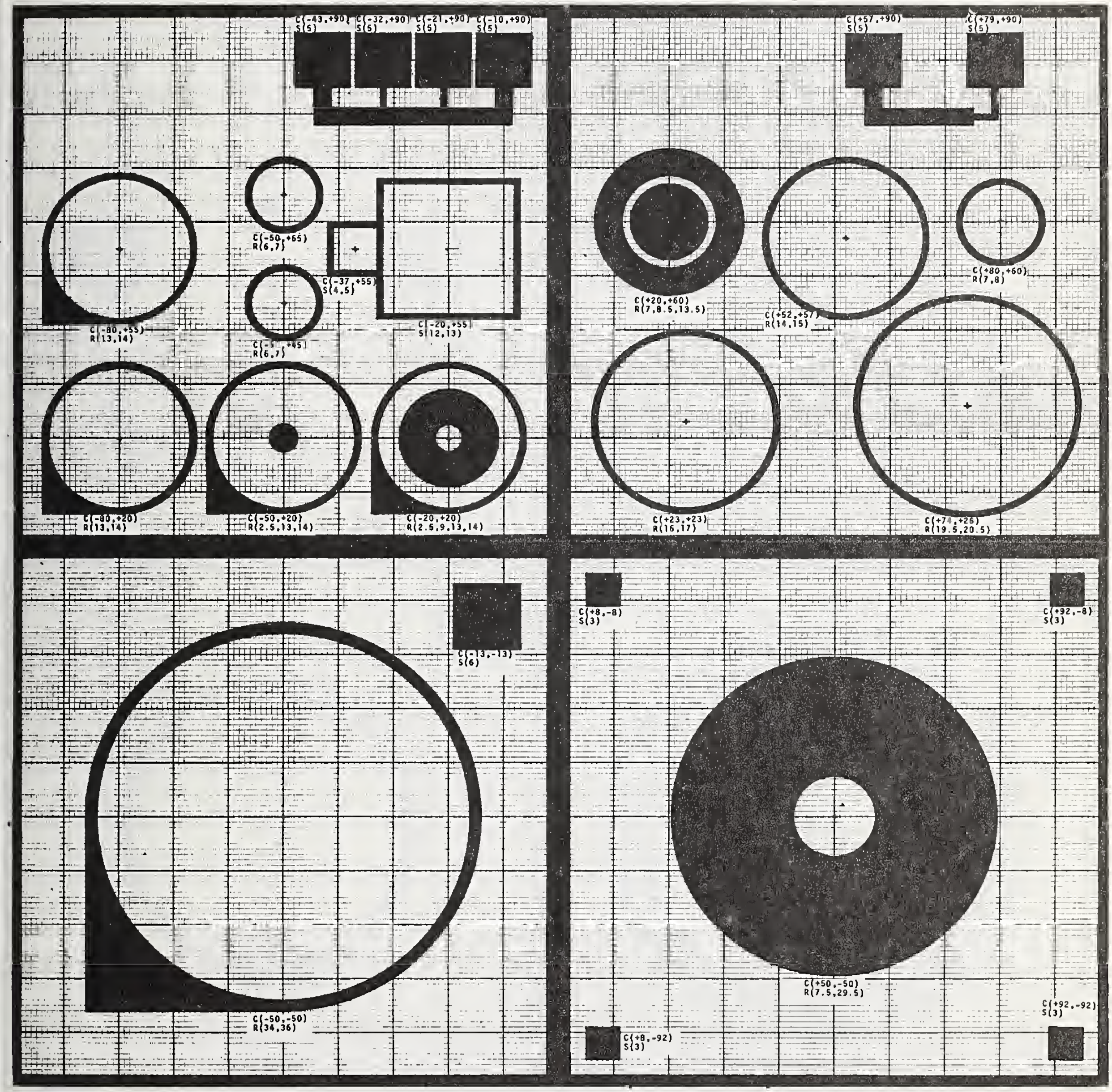
BASE MASK

(For positive photoresist black areas are clear on final mask)



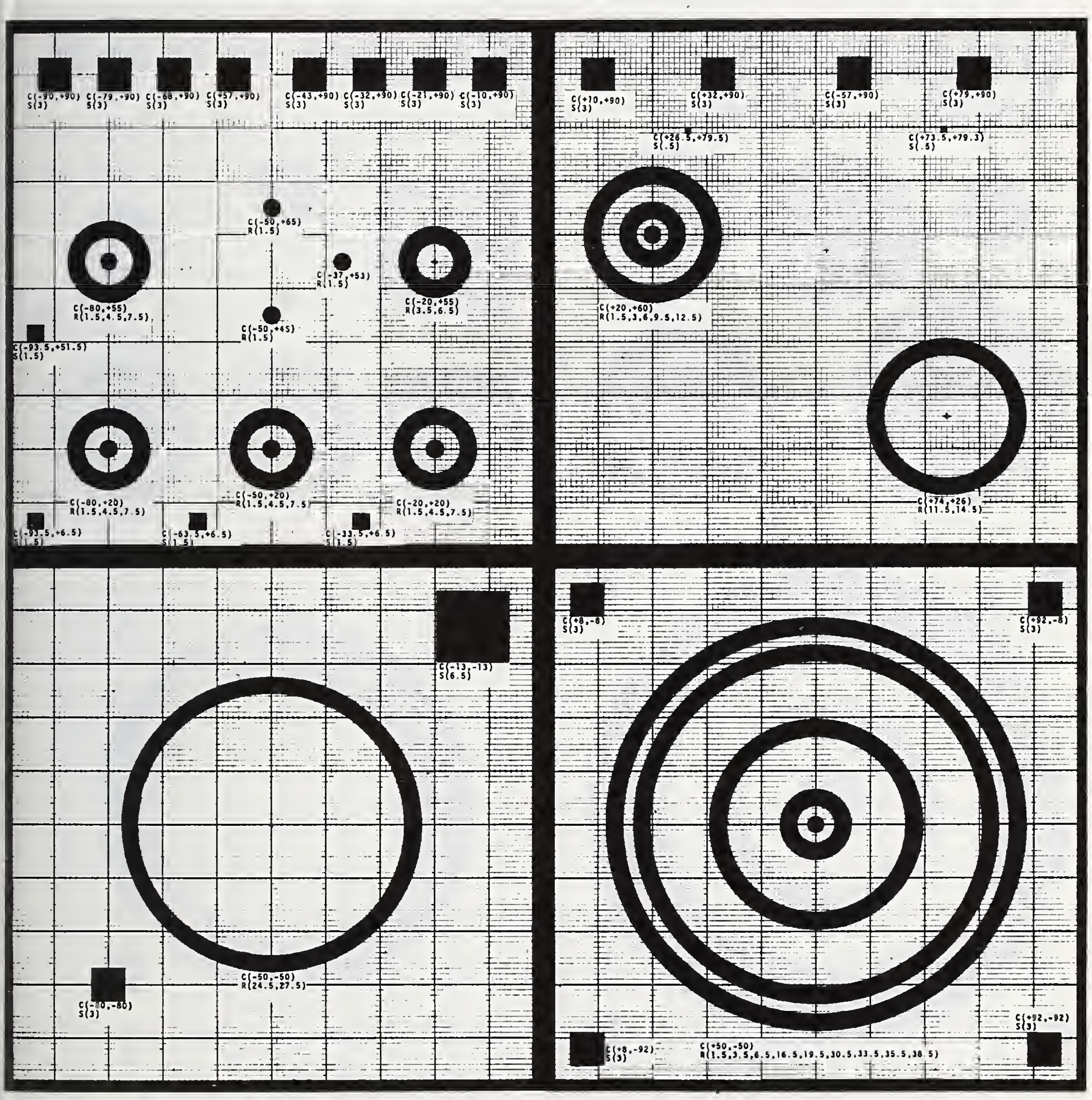
EMITTER MASK

(For positive photoresist black areas are clear on final mask)



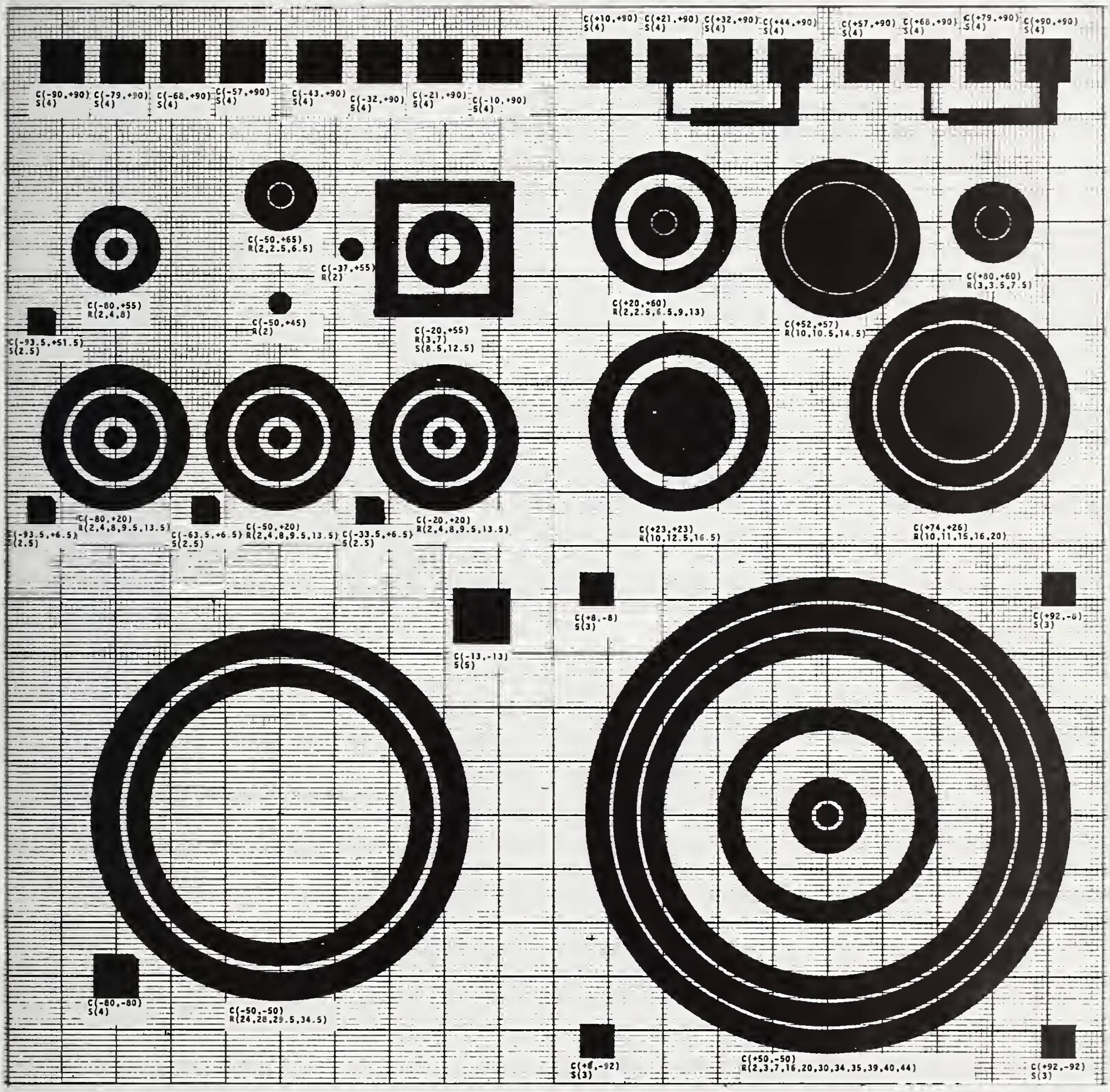
CONTACT MASK

(For positive photoresist black areas are clear on final mask)



METAL MASK

(For positive photoresist black areas are black on final mask)



NBS-114A (REV. 7-73)

U.S. DEPT. OF COMM. BIBLIOGRAPHIC DATA SHEET	1. PUBLICATION OR REPORT NO. NBS-SP-400-6	2. Gov't Accession No.	3. Recipient's Accession No.
4. TITLE AND SUBTITLE Microelectronic Test Patterns: An Overview			5. Publication Date August 1974
			6. Performing Organization Code
7. AUTHOR(S) Martin G. Buehler			8. Performing Organ. Report No.
9. PERFORMING ORGANIZATION NAME AND ADDRESS NATIONAL BUREAU OF STANDARDS DEPARTMENT OF COMMERCE WASHINGTON, D.C. 20234			10. Project/Task/Work Unit No.
			11. Contract/Grant No.
12. Sponsoring Organization Name and Complete Address (*Street, City, State, ZIP*) Defense Advanced Research Projects Agency - 1400 Wilson Blvd., Arlington, Virginia 22209 Defense Nuclear Agency - Washington, D. C. 20305 National Bureau of Standards, Washington, D. C. 20234			13. Type of Report & Period Covered Summary Report
			14. Sponsoring Agency Code

15. SUPPLEMENTARY NOTES

Library of Congress Catalog Card Number: 74-13001

16. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)*

The test patterns considered are those designed by the physical electronics engineer to evaluate fabrication processes rather than those designed by the microcircuit designer. The evaluation of fabrication processes can reveal if a process is under control and can indicate the stability and reliability of the resulting microcircuit. This evaluation is in essence an evaluation of a microcircuit's material characteristics, for process control and reliability depend ultimately on the right atoms being in the right places.

Various material analysis test structures are described, such as resistors, MOS capacitors, and gated *p-n* junctions along with the material parameters that can be derived from each. These test structures are illustrated by the NBS-2 test pattern, and its use in process control is described. Examples are given which span the range from those structures which are amenable to production testing to those which require an advanced measurement capability. In addition test structures are discussed with regard to their usability; this encompasses their size, sensitivity, correlation, contacting schemes, testability, and packaging. Test structures must be properly designed so that desired parameters are measured. In this regard various design aspects such as metal taps and diffused taps are mentioned. Finally the role of NBS in evaluating and designing test patterns is discussed.

17. KEY WORDS *(six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons)*

Integrated circuits; microelectronic test patterns.

18. AVAILABILITY [x] Unlimited	19. SECURITY CLASS (THIS REPORT)	21. NO. OF PAGES
[ ] For Official Distribution. Do Not Release to NTIS	UNCLASSIFIED	24
[x] Order From Sup. of Doc., U.S. Government Printing Office Washington, D.C. 20402, SD Cat. No. C13.10:400-6	20. SECURITY CLASS (THIS PAGE)	22. Price
[ ] Order From National Technical Information Service (NTIS) Springfield, Virginia 22151	UNCLASSIFIED	60 cents

USCOMM-DC 29042-P74

U.S. GOVERNMENT PRINTING OFFICE: 1974— 583-010:5

NBS TECHNICAL PUBLICATIONS

PERIODICALS

JOURNAL OF RESEARCH reports National Bureau of Standards research and development in physics, mathematics, and chemistry. Comprehensive scientific papers give complete details of the work, including laboratory data, experimental procedures, and theoretical and mathematical analyses. Illustrated with photographs, drawings, and charts. Includes listings of other NBS papers as issued.

Published in two sections, available separately:

- Physics and Chemistry (Section A)

Papers of interest primarily to scientists working in these fields. This section covers a broad range of physical and chemical research, with major emphasis on standards of physical measurement, fundamental constants, and properties of matter. Issued six times a year. Annual subscription: Domestic, $17.00; Foreign, $21.25.

- Mathematical Sciences (Section B)

Studies and compilations designed mainly for the mathematician and theoretical physicist. Topics in mathematical statistics, theory of experiment design, numerical analysis, theoretical physics and chemistry, logical design and programming of computers and computer systems. Short numerical tables. Issued quarterly. Annual subscription: Domestic, $9.00; Foreign, $11.25.

DIMENSIONS/NBS (formerly Technical News Bulletin)—This monthly magazine is published to inform scientists, engineers, businessmen, industry, teachers, students, and consumers of the latest advances in science and technology, with primary emphasis on the work at NBS.

DIMENSIONS/NBS highlights and reviews such issues as energy research, fire protection, building technology, metric conversion, pollution abatement, health and safety, and consumer product performance. In addition, DIMENSIONS/NBS reports the results of Bureau programs in measurement standards and techniques, properties of matter and materials, engineering standards and services, instrumentation, and automatic data processing.

Annual subscription: Domestic, $6.50; Foreign, $8.25.

NONPERIODICALS

Monographs—Major contributions to the technical literature on various subjects related to the Bureau's scientific and technical activities.

Handbooks—Recommended codes of engineering and industrial practice (including safety codes) developed in cooperation with interested industries, professional organizations, and regulatory bodies.

Special Publications—Include proceedings of high-level national and international conferences sponsored by NBS, precision measurement and calibration volumes, NBS annual reports, and other special publications appropriate to this grouping such as wall charts and bibliographies.

Applied Mathematics Series—Mathematical tables, manuals, and studies of special interest to physicists, engineers, chemists, biologists, mathematicians, computer programmers, and others engaged in scientific and technical work.

National Standard Reference Data Series—Provides quantitative data on the physical and chemical properties of materials, compiled from the world's literature and critically evaluated. Developed under a world-wide program coordinated by NBS. Program under authority of National Standard Data Act (Public Law 90-396). See also Section 1.2.3.

Building Science Series—Disseminates technical information developed at the Bureau on building materials, components, systems, and whole structures. The series presents research results, test methods, and performance criteria related to the structural and environmental functions and the durability and safety characteristics of building elements and systems.

Technical Notes—Studies or reports which are complete in themselves but restrictive in their treatment of a subject. Analogous to monographs but not so comprehensive in scope or definitive in treatment of the subject area. Often serve as a vehicle for final reports of work performed at NBS under the sponsorship of other government agencies.

Voluntary Product Standards—Developed under procedures published by the Department of Commerce in Part 10, Title 15, of the Code of Federal Regulations. The purpose of the standards is to establish nationally recognized requirements for products, and to provide all concerned interests with a basis for common understanding of the characteristics of the products. The National Bureau of Standards administers the Voluntary Product Standards program as a supplement to the activities of the private sector standardizing organizations.

Federal Information Processing Standards Publications (FIPS PUBS)—Publications in this series collectively constitute the Federal Information Processing Standards Register. The purpose of the Register is to serve as the official source of information in the Federal Government regarding standards issued by NBS pursuant to the Federal Property and Administrative Services Act of 1949 as amended, Public Law 89-306 (79 Stat. 1127), and as implemented by Executive Order 11717 (38 FR 12315, dated May 11, 1973) and Part 6 of Title 15 CFR (Code of Federal Regulations). FIPS PUBS will include approved Federal information processing standards information of general interest, and a complete index of relevant standards publications.

Consumer Information Series—Practical information, based on NBS research and experience, covering areas of interest to the consumer. Easily understandable language and illustrations provide useful background knowledge for shopping in today's technological marketplace.

NBS Interagency Reports—A special series of interim or final reports on work performed by NBS for outside sponsors (both government and non-government). In general, initial distribution is handled by the sponsor; public distribution is by the National Technical Information Service (Springfield, Va. 22151) in paper copy or microfiche form.

Order NBS publications (except Bibliographic Subscription Services) from: Superintendent of Documents, Government Printing Office, Washington, D.C. 20402.

BIBLIOGRAPHIC SUBSCRIPTION SERVICES

The following current-awareness and literature-survey bibliographies are issued periodically by the Bureau:

Cryogenic Data Center Current Awareness Service (Publications and Reports of Interest in Cryogenics). A literature survey issued weekly. Annual subscription: Domestic, $20.00; foreign, $25.00.

Liquefied Natural Gas. A literature survey issued quarterly. Annual subscription: $20.00.

Superconducting Devices and Materials. A literature survey issued quarterly. Annual subscription: $20.00. Send subscription orders and remittances for the preceding bibliographic services to the U.S. Department of Commerce, National Technical Information Service, Springfield, Va. 22151.

Electromagnetic Metrology Current Awareness Service (Abstracts of Selected Articles on Measurement Techniques and Standards of Electromagnetic Quantities from D-C to Millimeter-Wave Frequencies). Issued monthly. Annual subscription: $100.00 (Special rates for multi-subscriptions). Send subscription order and remittance to the Electromagnetic Metrology Information Center, Electromagnetics Division, National Bureau of Standards, Boulder, Colo. 80302.

U.S. DEPARTMENT OF COMMERCE
National Bureau of Standards
Washington, D.C. 20234

OFFICIAL BUSINESS

Penalty for Private Use, $300

POSTAGE AND FEES PAID
U.S. DEPARTMENT OF COMMERCE
COM-215